Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please withdraw claims 13-16, 18, 23, 28, 30-47, 51, 53, 57 and 69-73 from consideration.

1. (original) A circuit, comprising:

a high side switch coupled between an input and a load; and

a control circuit coupled to the high side switch, the control circuit adapted to control the high side switch as a function of a voltage across the high side switch.

2. (original) The circuit of claim 1 wherein the control circuit is adapted to turn the high side switch on for an on time period when the control circuit senses the voltage across the high side switch crosses below a first threshold while the high side switch is off.

3. (original) The circuit of claim 2 wherein the on time period is substantially fixed.

4. (original) The circuit of claim 1 wherein the control circuit is adapted to turn off the high side switch before an end of an on time period if the control circuit senses that the voltage drop across the high side switch crosses above a second threshold.

5. (original) The circuit of claim 4 wherein the control circuit is adapted to turn off the high side switch for a minimum off time period before the control circuit turns the high side switch on again.

6. (original) The circuit of claim 2 wherein the control circuit is adapted to delay the high side switch from being turned on for a delay time after the voltage across the high side switch crosses below the first threshold while the high side switch is off.

7. (original) The circuit of claim 1 wherein the load comprises a transformer.

8. (original) The circuit of claim 7 wherein the transformer includes a winding, wherein the control circuit is coupled to the winding of the transformer.

9. (original) The circuit of claim 1 wherein the high side switch is included in an integrated circuit.

10. (original) The circuit of claim 9 wherein the integrated circuit comprises the control circuit.

11. (original) The circuit of claim 1 wherein the circuit is included in a power conversion circuit.

12. (original) The circuit of claim 1 wherein the high side switch is a metal oxide semiconductor field effect transistor (MOSFET).

13. (withdrawn) The circuit of claim 1 wherein the control circuit is adapted to turn the high side switch on for an on time period when the control circuit senses a change in a slope of the voltage across the high side switch over time while the high side switch is off.

14. (withdrawn) The circuit of claim 13 wherein the on time period is substantially fixed.

15. (withdrawn) The circuit of claim 14 wherein the change in the slope of the voltage across the high side switch over time represents a change in a polarity of the slope of the voltage across the high side switch over time.

16. (withdrawn) The circuit of claim 13 wherein the control circuit is adapted to turn off the high side switch before an end of an on time period if the control circuit senses that the voltage drop across the high side switch crosses above a second threshold.

17. (original) The circuit of claim 1 wherein the control circuit is adapted to keep the high side off switch for a minimum off time period following a turn off of the high side switch.

18. (withdrawn) The circuit of claim 13 wherein the control circuit is adapted to delay the high side switch from being turned on for a delay time after the change in the slope of the voltage across the high side switch over time while the high side switch is off.

19. (original) The circuit of claim 1 wherein the input comprises a positive input terminal and a negative input terminal, wherein the high side switch is coupled between the positive input terminal and the load, the circuit further comprising a low side switch coupled between the negative input terminal and the load.

20. (original) The circuit of claim 19 wherein the low side switch is coupled to a second control circuit wherein the second control circuit is adapted to control the low side switch as a function of a voltage across the low side switch.

21. (original) The circuit of claim 20 wherein the low side switch is turned on after a delay time for a low side on time period when the voltage across the low side switch crosses below a low side threshold while the low side switch is off.

22. (original) The circuit of claim 21 wherein the delay time is substantially zero.

23. (withdrawn) The circuit of claim 21 further comprising a feedback circuit coupled between the load and the second control circuit to provide a feedback control loop, wherein the second control circuit is adapted to vary the delay time to regulate power delivered to the load.

24. (original) The circuit of claim 19 wherein the high side switch is turned on for a high side on time period when a voltage across the high side switch crosses below a high side threshold.

25. (original) The circuit in claim 24 wherein the low side switch is turned on after a delay time for a low side on time period when a voltage across the low side switch crosses below a low side threshold.

26. (original) The circuit of claim 25 wherein the high side on time period and the low side on time period are substantially fixed.

27. (original) The circuit of claim 25 wherein the high side on time period and low side on time periods are substantially equal.

28. (withdrawn) The circuit of claim 25 wherein the high side on time period is adjusted to maintain a voltage across the load during the high side on time period substantially equal to the voltage across the load during the low side on time period.

29. (original) The circuit of claim 25 wherein the delay time is substantially zero.

30. (withdrawn) The circuit of claim 19 wherein the high side switch is turned on for a high side on time period when a slope of a voltage across the high side switch changes while the high side switch is off.

31. (withdrawn) The circuit of claim 30 wherein the low side switch is turned on after a delay time for a low side on time period when a slope of a voltage across the low side switch changes while the low side switch is off.

32. (withdrawn) The circuit of claim 31 wherein the high side on time period and the low side on time period are substantially fixed.

33. (withdrawn) The circuit of claim 31 wherein the change in the slope of the voltage across the high side and low side switches is a change in a polarity of the slope across the high side and low side switches.

34. (withdrawn) The circuit of claim 31 wherein the high side on time period and low side on time periods are substantially equal.

35. (withdrawn) The circuit of claim 31 wherein the high side on time period is adjusted to maintain a voltage across the load during the high side on time period substantially equal to the voltage across the load during the low side on time period.

36. (withdrawn) The circuit of claim 35 wherein the voltage across the load during the high side on time period is sensed after a delay from the start of the high side on time period.

37. (withdrawn) The circuit of claim 35 wherein the voltage across the load during the low side on time period is sensed after a delay from the start of the low side on time period.

38. (withdrawn) The circuit of claim 31 wherein the delay time is substantially zero.

39. (withdrawn) The circuit of claim 31 further comprising a feedback circuit coupled between the load and the second control circuit to provide a feedback control loop, wherein the second control circuit is adapted to vary the delay time to regulate power delivered to the load.

40. (withdrawn) The circuit of claim 31wherein the low side switch is included in a low side integrated circuit.

41. (withdrawn) The circuit of claim 40 wherein the low side integrated circuit further comprises the second control circuit to generate the low side on time period.

42. (withdrawn) The circuit of claim 40 wherein the low side integrated circuit also comprises a sense circuit to sense a turn off of the high side switch.

43. (withdrawn) The circuit of claim 42 wherein the sense circuit senses the turn off of the high side switch by monitoring the voltage across the low side switch.

44. (withdrawn) The circuit of claim 30 wherein the high side switch is included in a high side integrated circuit.

45. (withdrawn) The circuit of claim 44 wherein the high side integrated circuit further comprises the control circuit to generate the high side on time period.

46. (withdrawn) The circuit of claim 45 wherein the high side integrated circuit also comprises a sense circuit to sense a turn off of the high side switch.

47. (withdrawn) The circuit of claim 46 wherein the sense circuit senses the turn off of the low side switch by monitoring the voltage across the high side switch.

48. (original) A half bridge circuit, comprising:

a low side switch;

a high side switch coupled to the low side switch;

a low side capacitor coupled to the low side switch;

a high side capacitor coupled to the low side capacitor and the high side switch; and

a load connected between a junction between the low side switch and high side switch and a junction between the low side capacitor and the high side capacitor, wherein the high side switch is adapted to be turned on for a high side on time period as a function of a voltage across the high side switch in response the low side switch turning off.

49. (original) The half bridge circuit of claim 48 wherein the low side switch is adapted to be turned on for a low side on time period following a delay time as a function of a voltage across the low side switch in response to the high side switch turning off.

50. (original) The circuit of 49 wherein the high side on time period and the low side on time period are substantially fixed.

51. (withdrawn) The circuit of claim 48 wherein the high side switch is adapted to be turned on for the high side on time period as a function of a slope of the voltage across the high side switch over time.

52. (original) The circuit of claim 48 wherein the high side switch is adapted to be turned on for the high side on time period when the voltage across the high side switch crosses below a first threshold while the high side switch is off.

53. (withdrawn) The half bridge circuit of claim 49 wherein one of the high side on time period or the low side on time period is adapted to be adjusted to maintain a voltage across the load during the high side on time period substantially equal to the voltage across the load during the low side on time period.

54. (original) The half bridge circuit of claim 48 wherein the voltage across the load is sensed for a fixed period during the high side on time period.

55. (original) The half bridge circuit of claim 49 wherein the voltage across the load is sensed for a fixed period during the low side on time period.

56. (original) The half bridge circuit of claim 49 wherein the delay time is substantially zero.

57. (withdrawn) The half bridge circuit of claim 49 further comprising a feedback circuit coupled between the load and the low side switch to vary the delay time to regulate power delivered to the load.

58. (original) The half bridge circuit of claim 49 wherein the low side switch is included in a low side integrated circuit of the half bridge circuit.

59. (original) The half bridge circuit of claim 58 wherein the low side integrated circuit also comprises a low side control circuit coupled to the low side switch to generate the low side on time period.

60. (original) The half bridge circuit of claim 59 where the low side control circuit is coupled to sense a turn off of the high side switch

61. (original) The half bridge circuit of claim 60 wherein the low side control circuit is adapted to sense the turn off of the high-side switch by monitoring the voltage across the low side switch

62. (original) The half bridge circuit of claim 48 wherein the high side switch is included in a high side integrated circuit of the half bridge circuit.

63. (original) The half bridge circuit of claim 62 wherein the high side integrated circuit also comprises a high side control circuit coupled to the high side switch to generate the high side on time period.

64. (original) The half bridge circuit of claim 63 wherein the high side control circuit is coupled to sense a turn off of the low side switch.

65. (original) The half bridge circuit of claim 64 wherein the high side control circuit is adapted to sense the turn off of the low side switch by monitoring the voltage across the high-side switch.

66. (original) The half bridge circuit of claim 49 wherein the half bridge circuit is included in a switched mode power supply.

67. (original) The half bridge circuit of claim 49 wherein the half bridge circuit is included in a power conversion circuit.

68. (original) The half bridge circuit of claim 49 wherein the low side switch and the high side switch each comprise a metal oxide field effect transistor (MOSFET).

69. (withdrawn) A circuit, comprising:

switching means coupled to a load for applying a voltage of a first polarity across the load during a first on time period and applying a voltage of the opposite polarity during a second on time period; and

sensing means coupled to the load for sensing the voltage across the load for a first sense period during the first on period and for a second sense period during the second on period, wherein the switching means is controlled to maintain a magnitude of the voltage across the load during the first on period substantially equal to the voltage across the load during the second on period.

70. (withdrawn) The circuit of claim 69 wherein the sensing means is adapted to generate a sense signal for a duration of the first and second sense periods.

71. (withdrawn) The circuit of claim 70 wherein a magnitude of the sense signal is adapted to be adjusted according to a magnitude of the voltage across the load during the first and second sense periods.

72. (withdrawn) The circuit of claim 71 wherein the sensing means comprises a capacitor and current charging means coupled to the capacitor for charging and discharging the capacitor.

73. (withdrawn) The circuit of claim 72 wherein the current charging means is adapted to adjust a current for charging and discharging the capacitor in response to the magnitude of the voltage across the load during the first and second sense periods.